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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,878	11/21/2003	Jeffrey S. Brown	5201-27900 03-0940	3082

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Leo Peters
LSI Logic Corporation
1621 Barber Lane, MS D-106
Milpitas, CA 95035

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,878	BROWN ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-20** are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 11/21/03 have been considered by the examiner (see attached PTO-1449).

Drawings

3. The drawings are objected to as failing to comply with 37CFR 1.84(p) (5) because they are informal drawing which are acceptable only for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1-2** are rejected under 35 U.S.C. **102(b)** as being clearly anticipated by Vlahos (U.S. PN: 5,231,598).

As per claim 1:

Vlahos teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of the comparator applied to a latch (50) (see col. 10, lines 15-36).

As per claim 2:

Vlahos teaches that the DUT (25) is a one pin to eight-pin clock driver circuit delivering eight secondary clock output signals at eight outputs (output terminals) of the device (see col. 9, lines 40-43).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims **3-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Vlahos (U.S. PN: 5,231,598) in view of Langford, II (U.S. PN: 6,671,860).

As per claims 3-5:

Vlahos teaches all subject matter claimed in claim 1 including a comparator (XOR gate) coupled to a latch. Vlahos does not explicitly teach a second logic gate (AND gate) coupled to receive signals and forwards an output signal to the logic gate (XOR). However, Langford teaches a boundary scan cell architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include an AND gate to the XOR gate as an input. This modification would have been obvious because a person having ordinary skill in the art would have been motivated operational signal to do so because providing an AND gate to the XOR circuit increases the test efficiency.

As per claims 6 and 7:

Vlahos teaches that subtracting the MAXCOUNT from the MAXNUM providing a skew number for the selected output signal for comparison with the skew numbers from other output signals of the DUT and the skew range or maximum output skew parameters are then determined from the respective skew numbers (see col. 5, lines 50-57)

9. Claims **8-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Vlahos (U.S. PN: 5,231,598) in view of Langford, II (U.S. PN: 6,671,860)

As per claims 8-9 and 12-15:

Vlahos teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of the comparator applied to a latch (50) (see col. 10, lines 15-36). Vlahos teaches all subject matter claimed in claim 1 including a comparator (XOR gate) coupled to a latch. Vlahos does not explicitly teach a second logic gate (AND gate) coupled to receive signals and forwards an output signal to the logic gate (XOR). Further, Vlahos teaches a skew tester (60) measures (delay measurement) output timing skew parameters OSHL and OSLH between multiple output signals of an integrated circuit (IC) device under test (DUT) having an input and multiple outputs (see abstract). However, Langford teaches a boundary scan cell architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include an AND gate to the XOR gate as an input. This modification would have been obvious because a person having ordinary skill in

the art would have been motivated operational signal to do so because providing an AND gate to the XOR circuit increases the test efficiency.

As per claims 10 and11:

Most of the limitations of this claim (8) have been noted in the rejections of claims 1 and 3 including Vlahos teaches that the microcontroller 12 may also be coupled to a conventional MCT (TM) Tester (MCT) for performing DC and AC function testing on a DUT in which case the skew testing circuit is disabled or transparent (see col. 7, lines 11-14).

As per claim 16-18

Vlahos teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of the comparator applied to a latch (50) (see col. 10, lines 15-36). Vlahos teaches all subject matter claimed in claim 1 including a comparator (XOR gate) coupled to a latch. Vlahos does not explicitly teach a second logic gate (AND gate) coupled to receive signals and forwards an output signal to the logic gate (XOR). Further, Vlahos teaches a skew tester (60) measures (delay measurement) output timing skew parameters OSHL and OSLH between multiple output signals of an integrated circuit (IC) device under test (DUT) having an input and multiple outputs (see abstract). However, Langford teaches a boundary scan cell

architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include an AND gate to the XOR gate as an input. This modification would have been obvious because a person having ordinary skill in the art would have been motivated operational signal to do so because providing an AND gate to the XOR circuit increases the test efficiency.

As per claims 19 and 20:

Most of the limitations of this claim (16) have been noted in the rejections of claims 1 and 3 including Vlahos teaches that the microcontroller 12 may also be coupled to a conventional MCT (TM) Tester (MCT) for performing DC and AC function testing on a DUT in which case the skew testing circuit is disabled or transparent (see col. 7, lines 11-14).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,594,797 Dudley et al.

US PN: 6,737,852 Soma et al.

US PN: 6,981,192 Pannis, Michael C.

US PN: 6,937,852 Pehrsson, Goran

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100